CLAIMS

1. (Canceled)

2. (Currently amended) The system of claim ~~1~~ 4 wherein the plurality of serial data channels includes a first, second, and third serial data channels;

wherein the plurality of parallel data channels includes a first, second, and third parallel data channels; and

wherein the serial to parallel converter is adapted to convert the serial data on the first, second, and third serial channels into corresponding parallel data on the first, second, and third parallel channels.

3. (Currently amended) The system of claim ~~1~~ 4 wherein the serial to parallel converter is adapted to generate a pixel clock for each parallel data channel and a parallel reference clock.

4. (Currently amended) ~~The~~ A system ~~of claim 3 wherein the alignment circuit comprises~~ to align digital image data, comprising:

a plurality of serial data channels, each channel transmitting corresponding serial data, the serial data on one serial channel having skew relative to the serial data on other serial channels;

a serial to parallel converter to convert the serial data on each of the plurality of serial data channels into parallel data on corresponding parallel data channels responsive to a serial reference clock and to generate a parallel reference clock responsive to the serial reference clock associated with the plurality of serial data channels;

a queue circuit ~~adapted~~ to store the parallel data on each of the parallel data channels responsive to a corresponding pixel clock; and

an alignment detection circuit ~~adapted~~ to detect alignment of the parallel data stored in the queue circuit responsive to the parallel reference clock.

5. (Currently amended) ~~The~~ A system ~~of claim 4~~ to align digital image data, comprising:

a plurality of serial data channels, each channel transmitting corresponding serial data, the serial data on one serial channel having skew relative to the serial data on other serial channels;

a serial to parallel converter to convert the serial data on each of the plurality of serial data channels into parallel data on corresponding parallel data channels responsive to a serial reference clock; and

an alignment circuit adapted to align the parallel data such that no skew is present between the parallel data on one parallel channel and the parallel data on other parallel channels responsive to a pixel clock;

wherein the serial to parallel converter generates a pixel clock for each parallel data channel and a parallel reference clock;

wherein the alignment circuit comprises:

a queue circuit to store the parallel data on each of the parallel data channels responsive to the corresponding pixel clock; and

an alignment detection circuit to detect alignment of the parallel data stored in the queue circuit responsive to the parallel reference clock; and

wherein the queue circuit for each of the parallel data channels comprises:

a plurality of FIFO latches, each FIFO latch ~~being adapted~~ to store ~~a word of~~ parallel data responsive to the corresponding pixel clock;

a compare circuit ~~adapted~~ to generate a match bit for each word of parallel data by monitoring the parallel data for a code;

a register circuit ~~adapted~~ to generate a leading edge signal responsive to the corresponding pixel clock;

a counter circuit ~~adapted~~ to generate a write pointer responsive to the corresponding pixel clock;

a latch circuit ~~adapted~~ to generate ~~the~~ a leading edge pointer by latching the write pointer responsive to the leading edge signal and the corresponding pixel clock; and

a multiplexer circuit ~~adapted~~ to receive parallel data stored in the plurality of FIFO latches and output aligned parallel data to a corresponding parallel data channel responsive to a corresponding read pointer.

6. (Currently amended) The system of claim 4 5

wherein each FIFO latch ~~is adapted to~~ stores a word of parallel data responsive to an enable signal; and

wherein the counter circuit ~~is further adapted to~~ generates the enable signal responsive to the corresponding pixel clock.

7. (Currently amended) The system of claim 6 wherein the counter circuit ~~is adapted to~~ generates the enable signal further responsive to a reset signal.

8. (Original) The system of claim 5 wherein the code is a blanking code.

9. (Currently amended) The system of claim 5 wherein the register circuit ~~is adapted to~~ generates the leading edge signal by comparing a match bit for a presently stored word of parallel data with a match bit for a previously stored word of parallel data.

10. (Currently amended) The system of claim 5 wherein the alignment detection circuit comprises:

an alignment detection block for each of the parallel data channels, each block ~~adapted~~ to generate the corresponding read pointer responsive to the parallel reference clock; and

a synchronization circuit ~~adapted~~ to receive a leading edge detect signal from each of the alignment detection blocks for each of the parallel data channels and generate a reload read pointer responsive to the parallel reference clock.

11. (Currently amended) The system of claim 10 wherein each alignment detection block comprises:

a shift circuit ~~adapted~~ to receive the corresponding leading edge pointer and generate the corresponding read pointer responsive to the reload read pointer;

a latch ~~adapted~~ to receive the leading edge signal and generate a leading edge detect signal for the corresponding parallel data channel responsive to the reload read pointer.

12. (Currently amended) The system of claim 11 wherein the shift circuit comprises:

a first multiplexer ~~adapted~~ to select between the corresponding leading edge pointer and corresponding read pointer responsive to the reload read pointer;

a shift register ~~adapted~~ to generate a shifted signal by shifting a first multiplexer output signal; and

a second multiplexer ~~adapted~~ to select between the first multiplexer output signal and the shifted output signal responsive to the reload read pointer.

13. (Currently amended) The system of claim ~~1~~ 4 further comprising a decoder adapted to receive the aligned parallel data on corresponding parallel channels from the alignment circuit, the decoder meeting the digital visual interface specification version 1.0.

14. (Currently amended) An alignment circuit receiving input parallel data on a plurality of input parallel data channels and generating output parallel data transmissible on a plurality of output parallel data channels, the input parallel data on one input parallel data channel having skew relative to the input parallel data on other input parallel data channels, comprising:

an alignment detection circuit ~~adapted~~ to generate a plurality of read pointers corresponding to the plurality of input parallel data channels responsive to a parallel reference clock signal; and

a plurality of FIFO circuits corresponding to the plurality of input parallel data channels ~~adapted~~ to generate the output parallel data responsive to the plurality of read pointers;

wherein the output data on one output channel has no skew relative to the output data on other output channels.

15. (Currently amended) The alignment circuit of claim 14 wherein the alignment detection circuit comprises an alignment detection block for each input data channel, each alignment detection block ~~adapted~~ to generate a read pointer for each input data channel responsive to the parallel reference clock.

16. (Currently amended) The alignment circuit of claim 15 wherein each alignment detection block comprises:

a read pointer generating circuit ~~adapted~~ to receive a corresponding leading edge pointer and generate the corresponding read pointer responsive to a reload read pointer signal;

a latch ~~adapted~~ to receive a leading edge signal and generate a leading edge detect signal for the corresponding input data channel responsive to the reload read pointer signal.

17. (Currently amended) ~~The~~ An alignment circuit ~~of claim 15~~ receiving input data on a plurality of input data channels and generating output data transmissible on a plurality of output data channels, the input data on one input data channel having skew relative to the input data on other input data channels, comprising:

an alignment detection circuit to generate a plurality of read pointers corresponding to the plurality of input data channels responsive to a reference clock signal; and

a plurality of FIFO circuits corresponding to the plurality of input data channels to generate the output data responsive to the plurality of read pointers;

wherein the output data on one output channel has no skew relative to the output data on other output channels;

wherein the alignment detection circuit comprises an alignment detection block for each input data channel, each block to generate a read pointer for each input data channel responsive to the parallel reference clock;

wherein the read pointer generating circuit comprises:

a first multiplexer ~~adapted~~ to multiplex between the corresponding leading edge pointer and corresponding read pointer responsive to the reload read pointer;

a shift circuit ~~adapted~~ to generate a shifted signal by shifting a first multiplexer output signal; and

a second multiplexer ~~adapted~~ to multiplex between the first multiplexer output signal and the shifted output signal responsive to the reload read pointer.

18. (Currently amended) The alignment circuit of claim 16 wherein the alignment detection circuit further comprises a feedback circuit ~~adapted~~ to generate the reload read pointer signal responsive to the parallel reference clock.

19. (Currently amended) The alignment circuit of claim 18 wherein the feedback circuit comprises:

a logic gate ~~adapted~~ to generate a logic gate signal by logically manipulating leading edge detect signals from each input data channel;

a plurality of serially connected registers ~~adapted~~ to generate the reload read pointer signal by registering the logic gate signal responsive to the parallel reference clock.

20. (Currently amended) The alignment circuit of claim 14 wherein each FIFO circuit comprises:

a plurality of FIFO latches, each FIFO latch ~~adapted~~ to store a word of input data responsive to a corresponding pixel clock;

a compare circuit ~~adapted~~ to generate a match bit for each word of input data by monitoring the input data for a code;

a register circuit ~~adapted~~ to generate a leading edge signal responsive to the corresponding pixel clock;

a counter circuit ~~adapted~~ to generate a write pointer responsive to the corresponding pixel clock;

a latch circuit ~~adapted~~ to generate a leading edge pointer by latching the write pointer responsive to the leading edge signal and the corresponding pixel clock; and

a multiplexer circuit ~~adapted~~ to receive input data stored in the plurality of FIFO latches and output aligned input data to a corresponding input data channel responsive to a corresponding read pointer.

21. (Original) The alignment circuit of claim 20 wherein the code is a DVI blanking code.

22. (Currently amended) The alignment circuit of claim 20 wherein the counter circuit ~~is adapted to~~ generates an enable signal responsive to the corresponding pixel clock and a reset signal and wherein each FIFO latch is enabled by the enable signal.

23. (Currently amended) The alignment circuit of claim 20 wherein the logic circuit ~~is adapted to~~ generates the leading edge signal by logically manipulating the match bit of a presently stored data word with a match bit of a previously stored data word responsive to corresponding pixel clock.

24. (Currently amended) An alignment circuit adapted to align input data transmitted on a corresponding plurality of input data channels, input data on one channel having skew relative to input data on other channels and relative to a data clock, comprising:

a plurality of FIFO circuits ~~adapted~~ to receive input data from a corresponding plurality of input data channels, each FIFO circuit comprising:

a plurality of FIFO latches ~~adapted~~ to receive input data from one of the plurality of input data channels responsive to a corresponding pixel clock;

a compare circuit ~~adapted~~ to generate a match bit ~~for each word of input data~~ by monitoring the input data for a code;

a register circuit ~~adapted~~ to generate a leading edge signal responsive to the corresponding pixel clock and the match bit;

a counter circuit ~~adapted~~ to generate a write pointer responsive to the corresponding pixel clock;

a latch circuit ~~adapted~~ to generate a leading edge pointer by latching the write pointer responsive to the leading edge signal and the corresponding pixel clock; and

a multiplexer circuit ~~adapted~~ to receive data stored in the plurality of FIFO latches and output aligned data to a corresponding data channel responsive to a corresponding read pointer;

a plurality of alignment detection circuits corresponding to the plurality of input data channels, each alignment detection circuit comprising:

a first multiplexer ~~adapted~~ to multiplex between the leading edge pointer and read pointer responsive to the reload read pointer;

a shift circuit ~~adapted~~ to generate a shifted signal by shifting a first multiplexer output signal; and

a second multiplexer ~~adapted~~ to multiplex between the first multiplexer output signal and the shifted output signal responsive to the reload read pointer; and

a latch ~~adapted~~ to receive a leading edge signal and generate a leading edge detect signal for the corresponding input data channel responsive to ~~the~~ a reload read pointer; and

a feedback circuit ~~adapted~~ to generate the reload read pointer responsive to the leading edge signal generated by each alignment detection circuit for each of the plurality of data channels.

25. (Currently amended) A method for aligning parallel image data, comprising:

receiving the data on a plurality of channels, the data on one channel having skew relative to the data on another channel;

storing the data in a plurality of queues;

detecting a valid data transition by checking the data for a predetermined code;

setting a read pointer for each channel responsive to the valid data transition; and

aligning the data by reading the plurality of queues once the read pointers for each of the channels point to a valid data transition.

26. (Original) The method of claim 25 wherein receiving the data comprises:

receiving serial data on a plurality of serial channels;

converting the serial data to parallel data; and

providing the parallel data to a plurality of parallel channels.

27. (Original) The method of claim 25 wherein storing the data in a plurality of queues includes for each channel storing a word of data in a plurality of FIFO latches responsive to a corresponding pixel clock.

28. (Original) The method of claim 25 wherein detecting a valid data transition comprises scanning each word of data for the code.

29. (Original) The method of claim 28 wherein detecting a valid data transition comprises:

storing the code for a previous word of data;

storing the code for a present word of data; and

comparing the code for the previous with the code for the present word of data.

30. (Original) The method of claim 29 wherein detecting a valid data transition includes generating a leading edge signal as a result of comparing the code.

31. (Original) The method of claim 30 wherein detecting a valid data transition includes:

generating a write pointer responsive to the pixel clock; and

generating a leading edge pointer by latching the write pointer responsive to the leading edge signal and the pixel clock.

32. (Original) The method of claim 31 wherein setting the read pointer includes:

generating a reload read pointer by logically manipulating the leading edge signal from each data channel; and

latching the leading edge pointer responsive to the reload read pointer.

33. (Original) The method of claim 32 wherein aligning the data by reading the plurality of queues includes:

multiplexing data from the plurality of FIFO latches to a corresponding data channel responsive to the read pointer, wherein multiplexed data provided to one data channel is aligned relative to other multiplexed data provided to other data channels.